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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,760	02/23/2004	Erik Berg	BP 3067	2231

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EXAMINER	
KOSTAK, VICTOR R	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,760	BERG ET AL.	
	Examiner	Art Unit	
	Victor R. Kostak	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-13,16 and 20* is/are rejected.

7)☒ Claim(s) *7,8,14,15 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/23/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Easley et al. (6,259,482).

Easley discloses a digital BTSC compander system (noting particularly Figs. 5, 6 and 19), wherein the system includes matrixing stage 604 (Fig. 6) that provides digital audio L/R summation and L/R difference signals, and respective sum and difference processing channels, as shown. Associated circuitry including stages 540, 560 and 562 generate a pilot signal 564 characterized by a digital sinusoid (col. 21 lines 36-47 detailed in Fig. 19) and based on a reference clock that follows a two-state (on-off) curve (e.g. col. 21 lines 12-19). The audio sum and difference operate at a first sample rate to match the standard analog BTSC filter transform functions in amplitude phase (e.g. col. 7 lines 27-50; col. 11 lines 42-48; col. 12 lines 42-44), and the pilot generator operates at a frequency higher than the sum/difference audio components (e.g. col. 21 lines 11-17), which includes a multiple of the base horizontal frequency Fh (stage 550 in Fig. 5 generates s 5 x Fh carrier), thereby meeting claim 10.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easley et al.

Regarding claim 1, the discussion of the rejection of claim 10 is incorporated herein, wherein although Easley does not describe his phase generator as providing a rollover signal, it would have been obvious to one of ordinary skill in the art to consider the digital loop filter and associated PLL as being capable of providing a rollover signal since the data generated thereby is digital and therefore the phase increments range from maximum and minimum values that can logically be rolled over (as by an associated up/down counter).

As for claim 5, Easley discloses forming the system on a single chip (col. 22 lines 20-25).

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Easley et al. in view of Wong et al. (5,295,079).

Easley does not describe his digital loop filter in particular detail, so it would have been obvious to one of ordinary skill in the art to use any suitable hardware therefore that would provide adequate processing, such as that disclosed by Wong, who discloses a digital loop filter 14 (Fig. 2) that includes a proportional plus integrating section involving scaling that generates the sum of a linear term and an integer term (col. 3 line 14+).

4. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Easley et al. in view of Kingston et al. (5,060,180).

It would have been obvious to one of ordinary skill in the art to ensure that the loop filter of Easley does not exceed adequate signal levels, such as by including some type of saturator as

disclosed by Kingston (Fig. 4), who includes two programmable scaling stages in his digital loop filter to maintain adequate digital levels.

5. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Easley et al. and Wong et al., in view of Kingston et al. (5,060,180).

As mentioned previously, Easley does not describe his digital loop filter in particular detail. It would therefore have been obvious to one of ordinary skill in the art to use any suitable hardware therefore that would provide adequate processing, such as that disclosed by Wong, who discloses a digital loop filter 14 (Fig. 2) that includes a proportional plus integrating section involving scaling that generates the sum of a linear term and an integer term (col. 3 line 14+).

Moreover, it would also have been obvious to one of ordinary skill in the art to ensure that the loop filter of Easley does not exceed adequate signal levels, such as by including some type of saturator as disclosed by Kingston (Fig. 4), who includes two programmable scaling stages in his digital loop filter to maintain adequate digital levels.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Easley et al. in view of Foster (6,441,482).

It would have been obvious to one of ordinary skill in the art to use any well substrate material as the chip in Easley, such as CMOS, which Foster acknowledges is commonly used (col. 1 lines 10-20).

7. Claims 11, 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easley et al. in view of Elliott et al. (5,497,405).

As for claims 11 and 16, the circuit arrangement in Fig. 19 that generates a digital sine wave (mentioned above) whose frequency matches the repetition rate of an external reference signal Fh using an internal clock having a first predetermined rate. The arrangement includes the application of a two-state clock signal (based on the Fh signal) which circuitry includes two PLLs characterized by the inclusion of feedback loops (not shown in), the repetition rates equal to the Fh frequency. A digital loop filter within stage 550 generates an offset to an expected frequency of the digital sinusoid to generate a pilot phase signal, the loop filter generating a signal in the feedback loop shown, and the sinusoid is eventually retrieved (provided) as a signal composite with the output signal 572.

It would have been obvious to include phase accumulator logic as disclosed in the digital sine generator of Elliott (stage 32 in Fig. 2) to provide data usable in generating the sinusoid based on an extended range of phase values so dictated by the continuously applied input signal.

As for claim 20, the digital sinusoid is a BTSC pilot subcarrier that is locked to the Fh component sync signal of a video signal for transmission.

8. Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easley et al. in view of Phillips (3,989,931).

It would have been obvious to one of ordinary skill in the art to include an up/down counter associated with the digital phase detector since the output of the digital phase detector

involves digital values on which a digital logic device would accordingly operate on, the phase difference directions dictating the up/down counting, as disclosed by Phillips.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Easley et al. and Elliott et al. in view of Wong et al. and Kingston et al.

As mentioned previously, Easley does not describe his digital loop filter in particular detail. It would therefore have been obvious to one of ordinary skill in the art to use any suitable hardware therefore that would provide adequate processing, such as that disclosed by Wong, who discloses a digital loop filter 14 (Fig. 2) that includes a proportional plus integrating section involving scaling that generates the sum of a linear term and an integer term (col. 3 line 14+).

Moreover, it would also have been obvious to one of ordinary skill in the art to ensure that the loop filter of Easley does not exceed adequate signal levels, such as by including some type of saturator as disclosed by Kingston (Fig. 4), who includes two programmable scaling stages in his digital loop filter to maintain adequate digital levels.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Claims 7, 8, 14, 15 and 17-19 appear allowable over the prior art.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor R. Kostak whose telephone number is (571) 272-7348. The examiner can normally be reached on Monday - Friday from 6:30am-3:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David W. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, Virginia 22313-1450

Or faxed to:

(571) 273-8300

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Customer Service Office whose telephone number is (703) 308-HELP.

/Victor R. Kostak/
Primary Examiner
Art Unit 2622

VRK